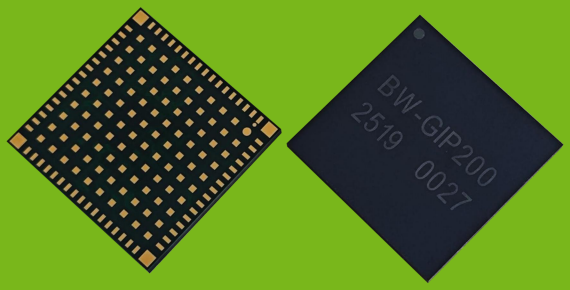


BW-GIP200 series

Seven-axis Integrated Navigation Microsystem

Technical Manual

V1.1

BW-GIP200

Seven-axis Integrated Navigation Microsystem

Product

BW-GIP200 is a chip-level packaged integrated navigation microsystem independently developed and designed by BWSENSING. It integrates a high-precision inertial measurement unit and satellite navigation, supports high-performance NRTK/PPP/PPP-RTK solutions, anti-interference, L-BAND PPP, integrated navigation, and other functions. It can provide continuous, real-time, and reliable high-precision position and attitude information in various harsh environments.
The microsystem also integrates an SOC chip with embedded integrated navigation algorithms, saving development time. Within its 25.0 mm x 24.4 mm dimensions, the GIP200 provides high reliability through its redundant design. Thanks to the integrated flash memory, the GIP200 also offers many additional features, such as support for firmware configurability and firmware upgrades.

Product

●System-level packaged integrated navigation chip

●Integrated satellite navigation chip and 6-axis inertial sensor

● Operating temperature: -40℃~+80℃

● ±16g accelerometer and three-axis ±4000°/s gyroscope

● GNSS and six-axis inertial sensor

● Cold start acquisition sensitivity: -147dBm

● Tracking sensitivity: -163dBm

● LGA80 package: 25.0mm×24.4mm×2 mm

Application

● Aircraft attitude and navigation

●Autonomousn driving integrated navigation

● Unmanned vehicle attitude and navigation

● Agricultural machinery and surveying and mapping

Dual Core Processor

• Dual-core 32-bit RISC-V processor, with a performance of up to 5.6 CoreMark/MHz, supports 32KB L1 instruction cache and 32KB L1 data cache, and supports 256 KB instruction local memory (ILM) and 256 KB data local memory (DLM).

• RV32-IMAFDCP instruction set: integer instruction set; multiplication instruction set; atomic instruction set; single-precision floating-point instruction set; double-precision floating-point instruction set; packed instruction set; DSP unit, supporting SIMD and DSP instructions, compatible with RV32-P extension instruction set.

memory

• On-chip SRAM: 2088 KB
• General-purpose registers: 64 bytes + 32 bytes
• Internal read-only memory ROM: 128KB
• One-time programmable memory OTP: 4096 bits

Two satellite navigation chips

The satellite navigation chip is an integrated BDS/GPS/GLONASS/Galileo/QZSS/SBAS/IRNSS satellite positioning, navigation, and timing RF baseband receiver chip, designed for global applications. It supports both multi-system joint positioning and single-system independent positioning modes, allowing users to flexibly configure and providing them with fast and accurate high-performance positioning services. The chip utilizes a 28nm process and an efficient PMU design, featuring miniaturization and low power consumption, significantly enhancing the endurance of user devices.

High-performance positioning and navigation system

✓ Supports four satellite systems: BDS, GPS, GLONASS, and Galileo
✓ Support SBAS
✓ Supports QZSS
✓ Support IRNSS
✓ Supports operation with individual systems of BDS, GPS, GLONASS, and Galileo
✓ Support dual-system operation
✓ Supports BDS/GPS/GLONASS, BDS/GPS/Galileo triple-system operation
✓ Supports the operation of BDS/GPS/Galileo/GLONASS systems
✓ The cold start acquisition sensitivity can reach -147 dBm, and the tracking sensitivity can reach -163 dBm
✓ Support anti-interference technology
✓ Support A-GNSS assisted positioning
✓ Support D-GNSS differential positioning

performance index

parameter	describe	performance index				notes
		minimum value	Typical values	Maximum value	unit	
Positioning accuracy 1 (Open land)	level		＜1		m	Default working mode
	elevation		＜2.5		m	
RTK positioning accuracy	level		1.5+1ppm		cm	
	elevation		2.0+1ppm		cm	
	B1/L1/E1 code		10		cm	
	B1/L1/E1 carrier phase		15		mm	

		performance index				
Observation accuracy	B2/L5/E5 code		10		cm	
	B2/L5/E5 carrier phase		15		mm	
	B3/L2 code		10		cm	
	B3/L3 carrier phase		15		mm	
Speed measurement accuracy 1			＜0.1		m/s	
First location time 2 TTFF	cold start		<28		s	
	hot start		1		s	
	Re capture		1		s	
Sensitivity 3	capture		-147		dBm	
	track		-163		dBm	
Serial port output baud rate		4800	230400	460800	bps	Default: 230400bps
Data update rate			1	20 (single mode) 10 (Third mold)	Hz	Default 1Hz
working voltage	VCC		3.3		V	
	V_BCKP		3.3		V	
Average Power			50		mA	The main power supply VCC is 3.3V
standby power			25		uA	Backup power supply 3.3V
External antenna gain				30	dB	
temperature	work	-40		85	℃	
	storage	-40		125	℃	
weight			＜1.5		g	

Note: 1. In an open and unobstructed scenario, the test antenna is a 25*25mm vehicular active antenna.

If there are more than 8 satellites, the strength of all satellites is -130dBm, PDOP is less than or equal to 5, and all time statistics are calculated as the average of 10 tests.

3. The external LNA has a noise figure of 0.8.

Six-axis IMU chip

The IMU chip is a high-performance 6-axis inertial sensor, consisting of a 16-bit digital three-axis ±16 g accelerometer and a 16-bit digital three-axis ±4000°/s gyroscope. It enables high-precision measurement of direction and motion detection along three orthogonal axes.

Measurement range and sensitivity

（A）:

±2 g： 0.061 mg/LSB

±4 g： 0.122 mg/LSB

±8 g： 0.244 mg/LSB

±16 g： 0.488 mg/LSB

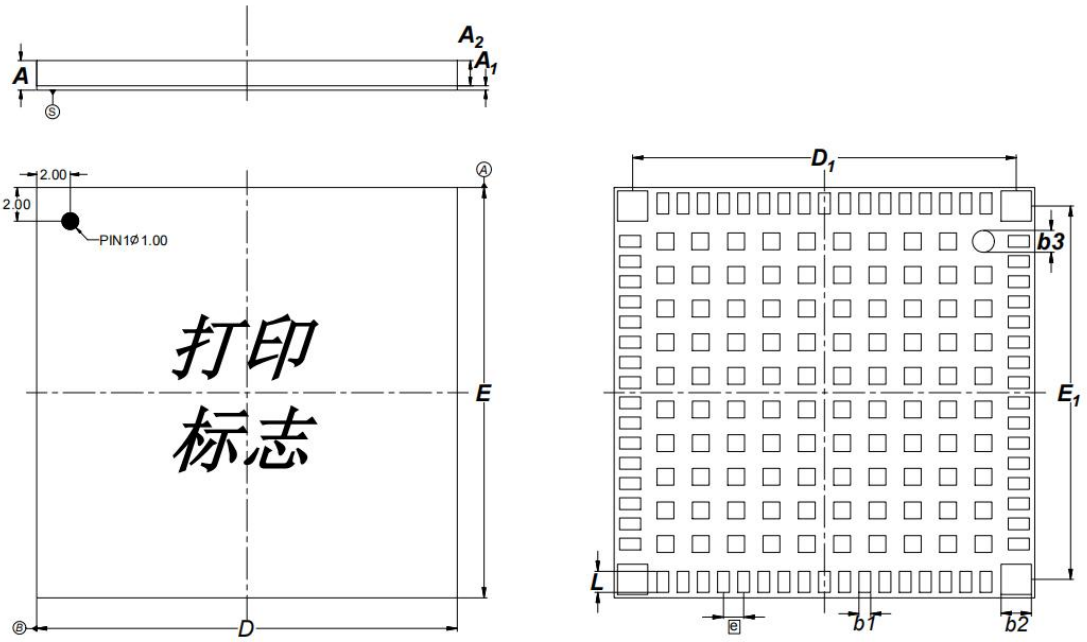
（G）:

±125 dps：4.37 mdps/LSB
±250 dps： 8.75 mdps/LSB
±500 dps： 17.5 mdps/LSB
±1000 dps： 35.0 mdps/LSB
±2000 dps： 70.0 mdps/LSB
±4000 dps： 140.0 mdps/LSB

performance index

IMU parameters		unit		
gyroscope	range	°/s		250
	angle random walk	°/√h		0.5
	Zero-bias instability	°/h		5
	Full temperature zero bias	°/s		0.3
	Scale error	-		4‰
	Three-axis orthogonal coupling error	-		1.7‰（0.1°）
accelerometer	range	g		±16
	rate random walk	m/s/√h		0.3
	Zero-bias instability	μg		50
	Full temperature zero bias	mg		5
	Scale error	-		2‰
	Three-axis orthogonal coupling error	-		0.9‰（0.05°）

Schematic diagram of



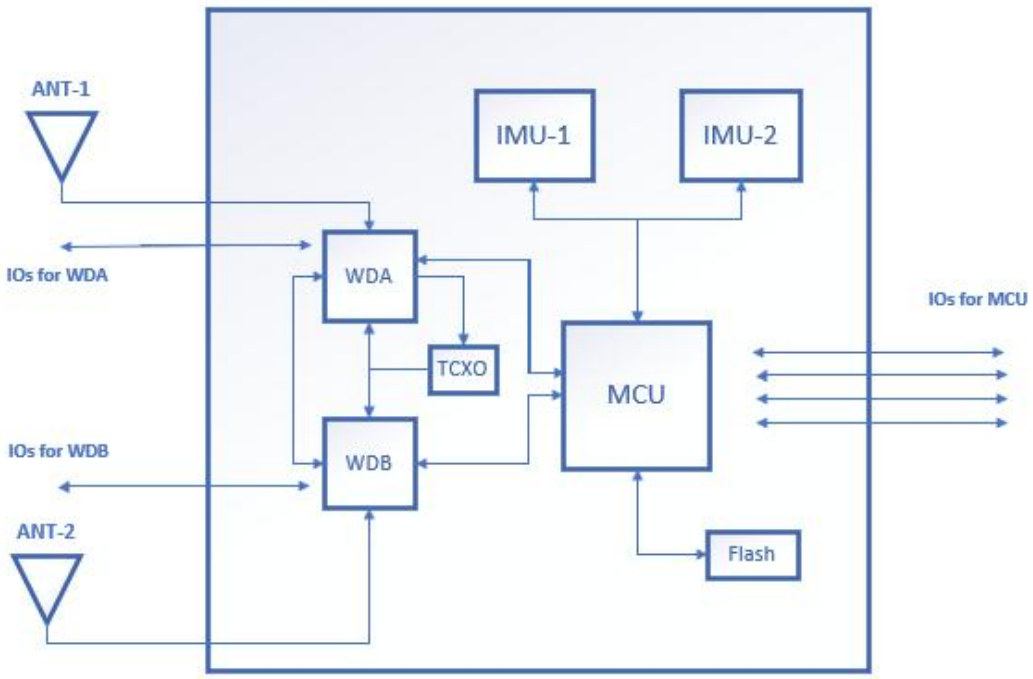
单位：mm

尺寸符号	最小值	公称值	最大值
A	1.67	1.76	1.85
A_1	0.23	0.26	0.29
A_2	-	1.50	-
b_1	-	0.70	-
b_2	-	1.80	-
b_3	-	1.30	-
D	24.90	25.00	25.10
D_1	-	22.80	-
E	24.30	24.40	24.50
E_1	-	22.20	-
e	-	1.20	-
L	-	1.25	-

备注：包封厚度 1.50 毫米。

Microsystem chip architecture

The architecture of the BW-GIP200 integrated navigation seven-axis microsystem chip is shown in the figure below

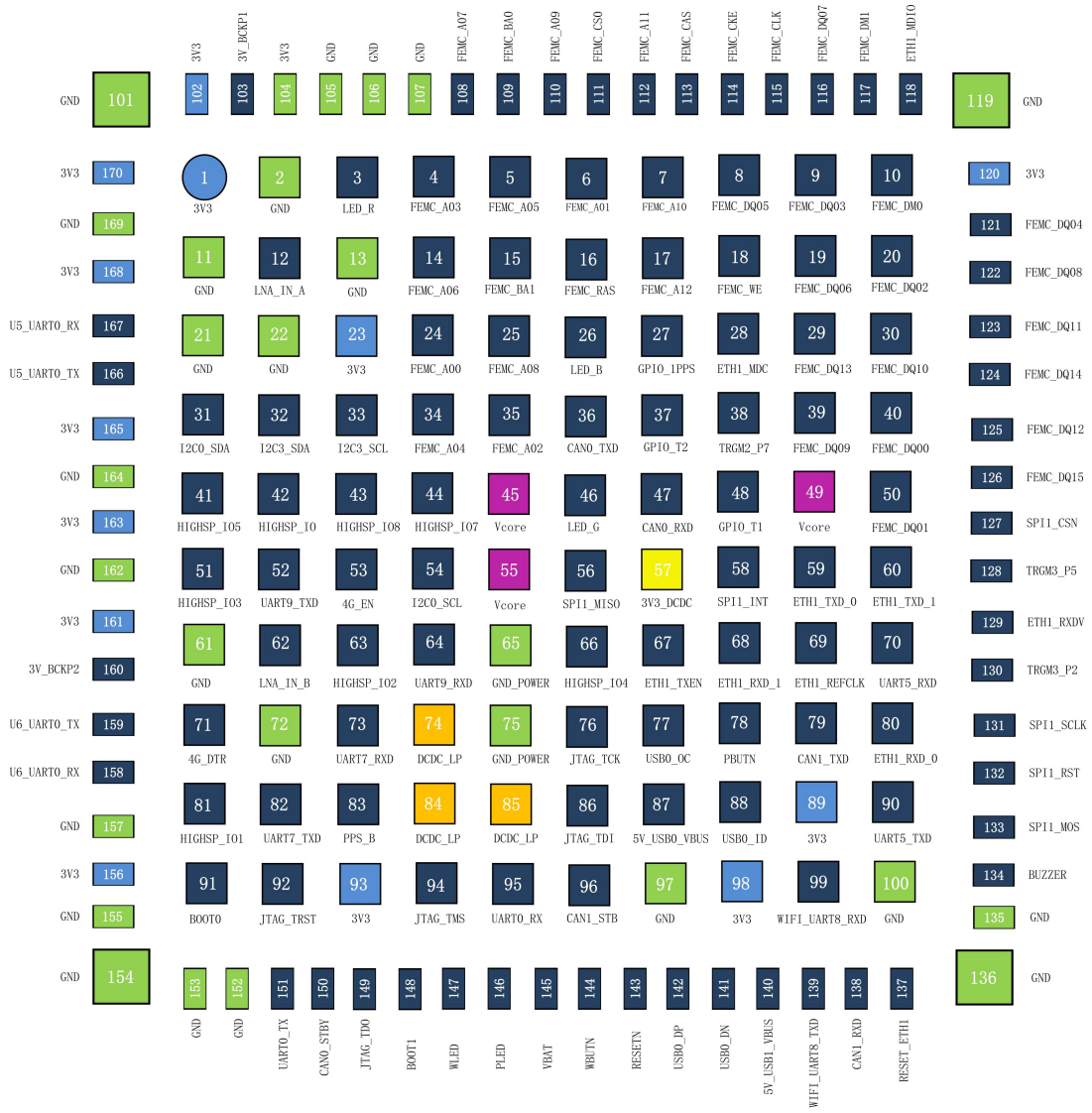


The internal interconnection table of the microsystem is as follows:

Chip 1	Chip 1 - Pin	Chip 2 - Pin	Chip 2	notes
WDA	GPIO17	GPIO19	WDB	Interconnected via UART
	GPIO19	GPIO17		
MCU	PE22	GPIO6	WDA	Interconnected via UART
	PE23	GPIO7		
MCU	PE27	GPIO6	WDB	Interconnected via UART
	PE28	GPIO7		
MCU	PB25	SDO	IMU-1/2	Interconnected via SPI
	PB21	SCL		
	PB22	SDA		
	PC01	CS	IMU-1	Film selection 1
	PC03	CS	IMU-2	Film selection 2
	PC20	INT1	IMU-1	Interrupt 1
	PD24	INT1	IMU-2	Interrupt 2

Pin Definition

Pin layout



Pin signal definition

Pin number	Pin Name	I/O	Digital function/description	Corresponding MCU pin	Corresponding to WDA pin	Corresponding to WDB pin
1	3V3	P				
2	GND	G				
3	LED_R	I/O	GPIO_B_18(ALT0)UART1_CTS(ALT3)CAN1_RXD(ALT7)DAOL_N(ALT10)FEMC_DQ_25(ALT12)PWM1_P_1(ALT16)	PB18		

4	FEMC_A03	I/O	GPIO_C_05(ALT0)UART10_TXD(ALT2)FEMC_A_03(ALT12)TRGM1_P_09(ALT16)	PC05		
5	FEMC_A05	I/O	GPIO_C_07(ALT0)UART8_TXD(ALT2)FEMC_A_05(ALT12)XPI1_CB_D_2(ALT14)TRGM0_P_02(ALT16)	PC07		
6	FEMC_A01	I/O	GPIO_C_09(ALT0)UART11_TXD(ALT2)FEMC_A_01(ALT12)XPI1_CB_CS1(ALT14)TRGM1_P_08(ALT16)ETH1_EVTO_0(ALT19)	PC09		
7	FEMC_A10	I/O	GPIO_C_15(ALT0)UART12_TXD(ALT2)FEMC_A_10(ALT12)XPI1_CB_SCLK(ALT14)TRGM1_P_06(ALT16)	PC15		
8	FEMC_DQ05	I/O	GPIO_C_27(ALT0)UART6_RXD(ALT2)FEMC_DQ_05(ALT12)PWM3_P_5(ALT16)ETH1_EVTO_2(ALT19)	PC27		
9	FEMC_DQ03	I/O	GPIO_D_01(ALT0)UART4_DE(ALT2)UART4_RTS(ALT3)I2C0_SCL(ALT4)FEMC_DQ_03(ALT12)PWM3_P_3(ALT16)ETH1_EVTO_1(ALT19)	PD01		
10	FEMC_DM0	I/O	GPIO_C_30(ALT0)UART3_RXD(ALT2)FEMC_DM_0(ALT12)XPI1_CB_CS0(ALT14)TRGM2_P_05(ALT16)	PC30		

11	GND	G				
12	LNA_IN_A	RF IO	An external 50 ohm impedance matching circuit is required		40 (LNA_IN)	
13	GND	G				
14	FEMC_A06	I/O	GPIO_C_10(ALT0)UART6_RXD(ALT2)FEMC_A_06(ALT12)XPI1_CB_CS0(ALT14)TRGM1_P_07(ALT16)	PC10		
15	FEMC_BA1	I/O	GPIO_C_14(ALT0)UART13_TXD(ALT2)FEMC_BA1(ALT12)XPI1_CB_DQS(ALT14)TRGM3_P_07(ALT16)ETH1_EVTO_1(ALT19)	PC14		
16	FEMC_RAS	I/O	GPIO_C_18(ALT0)UART1_RXD(ALT2)FEMC_RAS(ALT12)TRGM3_P_10(ALT16)	PC18		
17	FEMC_A12	I/O	GPIO_C_22(ALT0)UART15_TXD(ALT2)FEMC_A_12(ALT12)XPI1_CA_D_0(ALT14)TRGM2_P_00(ALT16)	PC22		
18	FEMC_WE	I/O	GPIO_C_24(ALT0)UART2_TXD(ALT2)FEMC_WE(ALT12)TRGM3_P_09(ALT16)ETH1_EVTI_1(ALT19)	PC24		
19	FEMC_DQ06	I/O	GPIO_C_28(ALT0)UART6_TXD(ALT2)FEMC_DQ_06(ALT12)PWM3_P_6(ALT16)ETH1_EVTO_0(ALT19)	PC28		

20	FEMC_DQ02	I/O	GPIO_D_00(ALT0)UART4_CTS(ALT3)I2C0_SDA(ALT4)FEMC_DQ_02(ALT12)PWM3_P_2(ALT16)	PD00		
21	GND	G				
22	GND	G				
23	3V3	P				
24	FEMC_A00	I/O	GPIO_C_08(ALT0)UART11_RXD(ALT2)FEMC_A_00(ALT12)TRGM1_P_10(ALT16)ETH1_EVTO_2(ALT19)	PC08		
25	FEMC_A08	I/O	GPIO_C_12(ALT0)UART9_TXD(ALT2)FEMC_A_08(ALT12)XPI1_CB_D_0(ALT14)TRGM0_P_01(ALT16)	PC12		
26	LED_B	I/O	GPIO_B_20(ALT0)UART3_CTS(ALT3)SPI2_DAT3(ALT5)CAN3_RXD(ALT7)FEMC_DQ_23(ALT12)PWM0_P_7(ALT16)	PB20		
27	GPIO_1PPS	I/O	GPIO_B_31(ALT0)UART5_RXD(ALT2)FEMC_DQ_18(ALT12)PWM0_P_2(ALT16)	PB31		
28	ETH1_MDC	I/O	GPIO_D_11(ALT0)UART8_CTS(ALT3)CAN0_RXD(ALT7)XPI1_CA_D_3(ALT14)PWM3_FAULT_1(ALT16)ETH1_MDC(ALT19)	PD11		

29	FEMC_DQ13	I/O	GPIO_D_09(ALT0)UART6_CTS(ALT3)I2C2_SDA(ALT4)CAN2_STBY(ALT7)FEMC_DQ_13(ALT12)XPI1_CA_DQS(ALT14)PWM2_P_5(ALT16)	PD09		
30	FEMC_DQ10	I/O	GPIO_D_07(ALT0)UART5_TXD(ALT2)FEMC_DQ_10(ALT12)XPI1_CB_D_2(ALT14)PWM2_P_2(ALT16)	PD07		
31	I2C0_SDA	I/O	GPIO_B_10(ALT0)UART12_CTS(ALT3)I2C0_SDA(ALT4)CAN3_STBY(ALT7)I2S3_BCLK(ALT8)TRGM1_P_04(ALT16)CAM1_XCLK(ALT22)	PB10		
32	I2C3_SDA	I/O	GPIO_B_13(ALT0)UART15_CTS(ALT3)I2C3_SDA(ALT4)CAN1_STBY(ALT7)I2S3_TXD_1(ALT8)TRGM1_P_03(ALT16)CAM1_D_8(ALT22)	PB13		
33	I2C3_SCL	I/O	GPIO_B_14(ALT0)UART15_DE(ALT2)UART15_RTS(ALT3)I2C3_SCL(ALT4)CAN0_STBY(ALT7)I2S3_TXD_0(ALT8)TRGM1_P_00(ALT16)CAM1_D_9(ALT22)	PB14		

34	FEMC_A04	I/O	GPIO_C_06(ALT0)UART8_RXD(ALT2)FEMC_A_04(ALT12)XPI1_CB_D_3(ALT14)TRGM0_P_04(ALT16)	PC06		
35	FEMC_A02	I/O	GPIO_C_04(ALT0)UART10_RXD(ALT2)FEMC_A_02(ALT12)TRGM1_P_11(ALT16)	PC04		
36	CAN0_TXD	I/O	GPIO_B_15(ALT0)UART0_DE(ALT2)UART0_RTS(ALT3)CAN0_TXD(ALT7)DAOR_P(ALT10)PWM0_FAULT_0(ALT16)SOC_REF0(ALT24)	PB15		
37	GPIO_T2	I/O	GPIO_C_00(ALT0)UART5_TXD(ALT2)FEMC_DQ_17(ALT12)PWM0_P_1(ALT16)	PC00		
38	TRGM2_P7	I/O	GPIO_D_20(ALT0)UART10_DE(ALT2)UART10_RTS(ALT3)CAN2_TXD(ALT7)TRGM2_P_07(ALT16)SDC1_DS(ALT17)ETH1_TXCK(ALT18)	PD20		
39	FEMC_DQ09	I/O	GPIO_D_03(ALT0)UART4_RXD(ALT2)FEMC_DQ_09(ALT12)XPI1_CB_D_1(ALT14)PWM2_P_1(ALT16)	PD03		

40	FEMC_DQ00	I/O	GPIO_D_08(ALT0)UART5_CTS(ALT3)I2C1_SDA(ALT4)FEMC_DQ_00(ALT12)XPI1_CA_CS1(ALT14)PWM3_P_0(ALT16)ETH1_EVTI_2(ALT19)	PD08		
41	HIGHSP_IO5	I/O	GPIO_B_02(ALT0)UART14_TXD(ALT2)I2S2_RXD_2(ALT8)I2S3_RXD_2(ALT9)PWM1_P_0(ALT16)DIS0_B_2(ALT20)SYSCTL_CLK_OBS_0(ALT24)	PB02		
42	HIGHSP_IO6	I/O	GPIO_B_05(ALT0)UART13_RXD(ALT2)I2S3_RXD_2(ALT8)I2S2_RXD_0(ALT9)TRGM0_P_08(ALT16)DIS0_B_0(ALT20)CAM1_D_6(ALT22)	PB05		
43	HIGHSP_IO8	I/O	GPIO_B_07(ALT0)UART15_TXD(ALT2)I2S3_RXD_0(ALT8)TRGM1_P_02(ALT16)DIS0_B_1(ALT20)CAM1_HSYNC(ALT22)SYSCTL_CLK_OBS_3(ALT24)	PB07		

44	HIGHSP_IO 7	I/O	GPIO_B_06(ALT0)UART1 5_RXD(ALT2)I2S3_RXD_ 1(ALT8)TRGM1_P_05(AL T16)DIS0_G_0(ALT20)CA M1_PIXCLK(ALT22)SYS CTL_CLK_OBS_2(ALT24)	PB06		
45	Vcore	P				
46	LED_G	I/O	GPIO_B_19(ALT0)UART1 _DE(ALT2)UART1_RTS(ALT3)CAN1_TXD(ALT7) FEMC_DQ_24(ALT12)PW M1_P_0(ALT16)	PB19		
47	CAN0_RXD	I/O	GPIO_B_17(ALT0)UART0 _CTS(ALT3)CAN0_RXD(ALT7)DAOL_P(ALT10)P WM0_FAULT_1(ALT16)	PB17		
48	GPIO_T1	I/O	GPIO_B_28(ALT0)UART0 _RXD(ALT2)SPI3_DAT2(ALT5)FEMC_DQ_19(ALT 12)PWM0_P_3(ALT16)	PB28		
49	Vcore	P				
50	FEMC_DQ0 1	I/O	GPIO_D_05(ALT0)UART5 _DE(ALT2)UART5_RTS(ALT3)I2C1_SCL(ALT4)FE MC_DQ_01(ALT12)PWM 3_P_1(ALT16)	PD05		
51	HIGHSP_IO 3	I/O	GPIO_B_00(ALT0)UART1 3_DE(ALT2)UART13_RT S(ALT3)I2C1_SCL(ALT4) SPI2_SCLK(ALT5)I2S3_T XD_2(ALT9)PWM0_P_2(ALT16)DIS0_R_2(ALT20)	PB00		

52	UART9_TXD	I/O	GPIO_A_30(ALT0)UART9_TXD(ALT2)CAN3_TXD(ALT7)I2S2_RXD_0(ALT8)I2S3_RXD_0(ALT9)PWM1_P_1(ALT16)DIS0_G_6(ALT20)CAM0_D_8(ALT22)	PA30		
53	4G_EN	I/O	GPIO_A_17(ALT0)GPTMR1_CAPT_0(ALT1)UART10_DE(ALT2)UART10_RTS(ALT3)CAN0_TXD(ALT7)I2S1_RXD_0(ALT9)DIS0_B_5(ALT20)CAM0_VSYNC(ALT22)	PA17		
54	I2C0_SCL	I/O	GPIO_B_11(ALT0)UART12_DE(ALT2)UART12_RTS(ALT3)I2C0_SCL(ALT4)CAN2_STBY(ALT7)I2S3_FCLK(ALT8)TRGM1_P_01(ALT16)CAM1_VSYNC(ALT22)	PB11		
55	Vcore	P				
56	SPI1_MISO	I/O	GPIO_D_30(ALT0)UART14_RXD(ALT2)SPI1_MISO(ALT5)CAN0_RXD(ALT7)XPI0_CB_D_2(ALT14)PWM2_P_1(ALT16)ETH0_RXDV(ALT18)	PD30		

57	3V3_DCDC	P				
58	SPI1_INT	I/O	GPIO_E_01(ALT0)UART12_TXD(ALT2)XPI0_CB_CS1(ALT14)PWM2_P_7(ALT16)SDC0_CDN(ALT17)ETH0_TXCK(ALT18)	PE01		
59	ETH1_TXD_0	I/O	GPIO_D_25(ALT0)UART10_CTS(ALT3)CAN2_RXD(ALT7)TRGM2_P_08(ALT16)SDC1_DATA_5(ALT17)ETH1_TXD_0(ALT18)	PD25		
60	ETH1_TXD_1	I/O	GPIO_D_16(ALT0)UART9_DE(ALT2)UART9_RTS(ALT3)CAN1_TXD(ALT7)TRGM2_P_06(ALT16)SDC1_DATA_4(ALT17)ETH1_TXD_1(ALT18)	PD16		
61	GND	G				
62	LNA_IN_B	RF IO	An external 50 ohm impedance matching circuit is required			40 (LNA_IN)
63	HIGHSP_IO2	I/O	GPIO_A_13(ALT0)GPTMR1_CAPT_0(ALT1)UART9_RTS(ALT3)I2C3_SCL(ALT4)SPI1_DAT2(ALT5)I2S1_RXD_2(ALT9)DIS0_B_6(ALT20)CAM0_HSYNC(ALT22)	PA13		

64	UART9_RXD	I/O	GPIO_A_29(ALT0)UART9_RXD(ALT2)CAN3_RXD(ALT7)I2S2_RXD_1(ALT8)I2S3_RXD_1(ALT9)PWM1_P_3(ALT16)DIS0_G_4(ALT20)CAM0_D_9(ALT22)	PA29		
65	GND_POWER	G				
66	HIGHSP_IO4	I/O	GPIO_B_01(ALT0)UART14_RXD(ALT2)I2S2_RXD_3(ALT8)I2S3_RXD_3(ALT9)PWM1_P_2(ALT16)DIS0_G_1(ALT20)SYSCTL_CLK_OBS_1(ALT24)	PB01		
67	ETH1_TXEN	I/O	GPIO_E_14(ALT0)GPTMR3_CAPT_0(ALT1)UART14_CTS(ALT3)I2C0_SDA(ALT4)I2S0_TXD_2(ALT8)PWM3_P_5(ALT16)SDC1_WP(ALT17)ETH1_TXEN(ALT18)	PE14		
68	ETH1_RXD_1	I/O	GPIO_E_18(ALT0)GPTMR2_COMP_0(ALT1)UART3_TXD(ALT2)I2S0_FCLK(ALT8)PWM3_P_7(ALT16)SDC0_CDN(ALT17)ETH1_RXD_1(ALT18)ETH0_EVTO_1(ALT19)	PE18		

69	ETH1_REFCLK	I/O	GPIO_E_16(ALT0)GPTMR2_COMP_1(ALT1)UART2_TXD(ALT2)I2S0_MCLK(ALT8)PWM3_P_3(ALT16)SDC1_VSEL(ALT17)ETH1_REFCLK(ALT18)	PE16		
70	UART5_RXD	I/O	GPIO_E_24(ALT0)GPTMR3_COMP_1(ALT1)UART5_RXD(ALT2)I2S0_RXD_2(ALT8)ACMP_COMP_2(ALT16)SOC_REF1(ALT24)	PE24		
71	4G_DTR	I/O	GPIO_A_16(ALT0)GPTMR1_CAPT_1(ALT1)UART10_CTS(ALT3)SPI1_MOSI(ALT5)CAN0_RXD(ALT7)I2S1_RXD_1(ALT9)DIS0_B_3(ALT20)CAM0_XCLK(ALT22)	PA16		
72	GND	G				
73	UART7_RXD	I/O	GPIO_A_10(ALT0)GPTMR0_COMP_1(ALT1)UART7_RXD(ALT2)I2C1_SDA(ALT4)CAN3_STBY(ALT7)I2S1_RXD_1(ALT8)DAOL_N(ALT10)CAM0_XCLK(ALT22)	PA10		
74	DCDC_LP	O		DCDC_LP		
75	GND_POWER	G				
76	JTAG_TCK	I/O	PGPIO_Y_02(ALT0)JTAG_TCK(ALT1)PTMR_COMP_2(ALT2)SOC_PY_02(ALT3)	PY02		

77	USB0_OC	I/O	GPIO_F_08(ALT0)GPTMR5_CAPT_0(ALT1)UART2_CTS(ALT3)I2C0_SDA(ALT4)I2S0_RXD_0(ALT9)USB0_OC(ALT24)	PF08		
78	PBUTN	I/O	BGPIO_Z_02(ALT0)PBUTN(ALT1)TAMP_02(ALT2)SOC_PZ_02(ALT3)	PZ02		
79	CAN1_TXD	I/O	GPIO_E_31(ALT0)UART7_TXD(ALT2)SPI2_CSN(ALT5)CAN1_TXD(ALT7)PDM0_CLK(ALT10)ETH0_REFCLK(ALT18)	PE31		
80	ETH1_RXD_0	I/O	GPIO_D_18(ALT0)UART11_DE(ALT2)UART11_RTS(ALT3)CAN3_TXD(ALT7)TRGM3_P_00(ALT16)SDC1_DATA_0(ALT17)ETH1_RXD_0(ALT18)	PD18		
81	HIGHSP_IO1	I/O	GPIO_A_12(ALT0)GPTMR1_CAPT_1(ALT1)UART9_CTS(ALT3)I2C3_SDA(ALT4)SPI1_DAT3(ALT5)I2S1_RXD_3(ALT9)DIS0_B_4(ALT20)CAM0_PIXCLK(ALT22)	PA12		
82	UART7_TXD	I/O	GPIO_A_11(ALT0)GPTMR0_COMP_0(ALT1)UART7_TXD(ALT2)I2C1_SCL(ALT4)CAN2_STBY(ALT7)I2S1_RXD_0(ALT8)DAOR_N(ALT10)CAM0_PIXCLK(ALT22)	PA11		

83	PPS_B	I/O	1. Default is Input, with internal pull-up. 2. Can be reused for other purposes. For details, see I/O reuse description			35 (GPIO11)
84	DCDC_LP	O		DCDC_LP		
85	DCDC_LP	O		DCDC_LP		
86	JTAG_TDI	I/O	PGPIO_Y_01(ALT0)JTAG_TDI(ALT1)PTMR_COMP_1(ALT2)SOC_PY_01(ALT3)	PY01		
87	5V_USB0_VBUS	I		USB0_VBUS		
88	USB0_ID	I/O	GPIO_F_10(ALT0)UART9_TXD(ALT2)I2C3_SCL(ALT4)SPI3_DAT2(ALT5)I2S0_TXD_0(ALT9)USB0_ID(ALT24)	PF10		
89	3V3	P				
90	UART5_TXD	I/O	GPIO_E_25(ALT0)GPTMR4_CAPT_1(ALT1)UART5_TXD(ALT2)I2S0_RXD_1(ALT8)ACMP_COMP_1(ALT16)ETH0_EVTI_1(ALT19)	PE25		
91	BOOT0	I/O	BGPIO_Z_06(ALT0)TAMP_06(ALT2)SOC_PZ_06(ALT3)	PZ06		
92	JTAG_TRST	I/O	PGPIO_Y_04(ALT0)JTAG_TRST(ALT1)PTMR_COMP_0(ALT2)SOC_PY_04(ALT3)	PY04		
93	3V3	P				

94	JTAG_TMS	I/O	PGPIO_Y_03(ALT0)JTAG_TMS(ALT1)PTMR_COMP_3(ALT2)SOC_PY_03(ALT3)	PY03		
95	UART0_RX	I/O	GPIO_Y_07(ALT0)UART0_RXD(ALT2)CAN1_RXD(ALT7)I2S1_BCLK(ALT8)	PY07		
96	CAN1_STBY	I/O	GPIO_Z_10(ALT0)GPTMR7_CAPT_1(ALT1)UART14_RXD(ALT2)I2C0_SDA(ALT4)CAN1_STBY(ALT7)ACMP_COMP_3(ALT16)	PZ10		
97	GND	G				
98	3V3	P				
99	WIFI_UART8_RXD	I/O	GPIO_F_06(ALT0)GPTMR5_CAPT_1(ALT1)UART8_RXD(ALT2)I2C2_SDA(ALT4)SPI3_MISO(ALT5)I2S0_BCLK(ALT9)ETH0_EVTO_1(ALT19)USB1_PWR(ALT24)	PF06		
100	GND	G				
101	GND	G				
102	3V3	P				
103	3V_BCKP1	I	It is advisable to externally connect a decoupling capacitor to the input terminal of the backup power supply, and during PCB layout , place the capacitor (>1uF) close to the corresponding pin		6 (VBCKP)	
104	3V3	P				
105	GND	G				
106	GND	G				
107	GND	G				

108	FEMC_A07	I/O	GPIO_C_11(ALT0)UART9_RXD(ALT2)FEMC_A_07(ALT12)XPI1_CB_D_1(ALT14)TRGM0_P_05(ALT16)	PC11		
109	FEMC_BA0	I/O	GPIO_C_13(ALT0)UART13_RXD(ALT2)FEMC_BA0(ALT12)	PC13		
110	FEMC_A09	I/O	GPIO_C_17(ALT0)UART14_TXD(ALT2)FEMC_A_09(ALT12)XPI1_CA_SCLK(ALT14)TRGM0_P_00(ALT16)	PC17		
111	FEMC_CS0	I/O	GPIO_C_19(ALT0)UART1_TXD(ALT2)FEMC_CS_0(ALT12)XPI1_CA_CS1(ALT14)TRGM3_P_08(ALT16)ETH1_EVTI_0(ALT19)	PC19		
112	FEMC_A11	I/O	GPIO_C_21(ALT0)UART15_RXD(ALT2)FEMC_A_11(ALT12)XPI1_CA_D_2(ALT14)TRGM2_P_03(ALT16)	PC21		
113	FEMC_CAS	I/O	GPIO_C_23(ALT0)UART2_RXD(ALT2)FEMC_CAS(ALT12)TRGM3_P_11(ALT16)ETH1_EVTI_2(ALT19)	PC23		
114	FEMC_CKE	I/O	GPIO_C_25(ALT0)UART0_RXD(ALT2)FEMC_CKE(ALT12)XPI1_CA_D_3(ALT14)TRGM2_P_04(ALT16)	PC25		

115	FEMC_CLK	I/O	GPIO_C_26(ALT0)UART0_TXD(ALT2)FEMC_CLK(ALT12)XPI1_CA_D_1(ALT14)TRGM2_P_01(ALT16)	PC26		
116	FEMC_DQ07	I/O	GPIO_C_29(ALT0)UART7_TXD(ALT2)FEMC_DQ_07(ALT12)XPI1_CB_CS1(ALT14)PWM3_P_7(ALT16)ETH1_EVTI_0(ALT19)	PC29		
117	FEMC_DM1	I/O	GPIO_C_31(ALT0)UART3_TXD(ALT2)FEMC_DM_1(ALT12)XPI1_CB_SCLK(ALT14)PWM2_FAULT_0(ALT16)	PC31		
118	ETH1_MDIO	I/O	GPIO_D_14(ALT0)UART8_DE(ALT2)UART8_RTS(ALT3)CAN0_TXD(ALT7)XPI1_CA_D_2(ALT14)PWM3_FAULT_0(ALT16)ETH1_MDIO(ALT19)	PD14		
119	GND	G				
120	3V3	P				
121	FEMC_DQ04	I/O	GPIO_D_02(ALT0)UART7_RXD(ALT2)FEMC_DQ_04(ALT12)XPI1_CB_DQS(ALT14)PWM3_P_4(ALT16)ETH1_EVTI_1(ALT19)	PD02		
122	FEMC_DQ08	I/O	GPIO_D_04(ALT0)UART4_TXD(ALT2)FEMC_DQ_08(ALT12)XPI1_CB_D_0(ALT14)PWM2_P_0(ALT16)	PD04		

123	FEMC_DQ11	I/O	GPIO_D_06(ALT0)UART5_RXD(ALT2)FEMC_DQ_11(ALT12)XPI1_CB_D_3(ALT14)PWM2_P_3(ALT16)	PD06		
124	FEMC_DQ14	I/O	GPIO_D_13(ALT0)UART7_DE(ALT2)UART7_RTS(ALT3)I2C3_SCL(ALT4)CAN1_STBY(ALT7)FEMC_DQ_14(ALT12)XPI1_CA_CS0(ALT14)PWM2_P_6(ALT16)	PD13		
125	FEMC_DQ12	I/O	GPIO_D_10(ALT0)UART6_DE(ALT2)UART6_RTS(ALT3)I2C2_SCL(ALT4)CAN0_STBY(ALT7)FEMC_DQ_12(ALT12)XPI1_CA_SCLK(ALT14)PWM2_P_4(ALT16)	PD10		
126	FEMC_DQ15	I/O	GPIO_D_12(ALT0)UART7_CTS(ALT3)I2C3_SDA(ALT4)CAN3_STBY(ALT7)FEMC_DQ_15(ALT12)XPI1_CA_D_1(ALT14)PWM2_P_7(ALT16)ETH0_MDC(ALT19)	PD12		
127	SPI1_CSN	I/O	GPIO_E_03(ALT0)UART15_RXD(ALT2)SPI1_CSN(ALT5)CAN1_RXD(ALT7)XPI0_CB_D_3(ALT14)PWM2_P_3(ALT16)ETH0_RXCK(ALT18)	PE03		

128	TRGM3_P5	I/O	GPIO_D_28(ALT0)UART11_RXD(ALT2)XPI0_CA_CS1(ALT14)PWM2_P_5(ALT16)SDC1_CDN(ALT17)ETH0_TXD_2(ALT18)	PD26		
129	ETH1_RXDV	I/O	GPIO_D_21(ALT0)UART8_RXD(ALT2)SPI0_MOSI(ALT5)TRGM3_P_04(ALT16)SDC1_CMD(ALT17)ETH1_RXDV(ALT18)	PD21		
130	TRGM3_P2	I/O	GPIO_D_27(ALT0)UART9_TXD(ALT2)SPI0_SCLK(ALT5)TRGM3_P_02(ALT16)SDC1_DATA_2(ALT17)ETH1_RXD_1(ALT18)	PD27		
131	SPI1_SCLK	I/O	GPIO_D_31(ALT0)UART14_TXD(ALT2)SPI1_SCLK(ALT5)CAN0_TXD(ALT7)XPI0_CB_D_0(ALT14)PWM2_P_0(ALT16)ETH0_RXD_0(ALT18)	PD31		
132	SPI1_RST	I/O	GPIO_E_02(ALT0)UART13_TXD(ALT2)SPI1_DAT2(ALT5)XPI0_CB_CS0(ALT14)PWM3_P_0(ALT16)ETH0_RXD_2(ALT18)	PE02		
133	SPI1_MOSI	I/O	GPIO_E_04(ALT0)UART15_TXD(ALT2)SPI1_MOSI(ALT5)CAN1_TXD(ALT7)XPI0_CB_D_1(ALT14)PWM2_P_2(ALT16)ETH0_RXD_1(ALT18)	PE04		

134	BUZZER	I/O	GPIO_E_05(ALT0)UART13_CTS(ALT3)CAN3_RXD(ALT7)PWM3_P_4(ALT16)SDC0_WP(ALT17)ETH0_TXD_3(ALT18)	PE05		
135	GND	G		PE05		
136	GND	G				
137	RESET_ETH1	I/O	GPIO_E_26(ALT0)UART1_DE(ALT2)UART1_RTS(ALT3)SPI2_DAT3(ALT5)CAN3_TXD(ALT7)I2S0_RXD_0(ALT8)SDC0_DATA_0(ALT17)ETH0_TXEN(ALT18)	PE26		
138	CAN1_RXD	I/O	GPIO_E_30(ALT0)UART7_RXD(ALT2)SPI2_MOSI(ALT5)CAN1_RXD(ALT7)PDM0_D_0(ALT10)USB1_OC(ALT24)	PE30		
139	WIFI_UART8_TXD	I/O	GPIO_F_07(ALT0)UART8_TXD(ALT2)I2C2_SCL(ALT4)SPI3_MOSI(ALT5)I2S0_TXD_1(ALT9)PDM0_CLK(ALT10)USB1_ID(ALT24)	PF07		
140	5V_USB1_VBUS	I		USB1_VBUS		
141	USB0_DN	I/O		USB0_DN		
142	USB0_DP	I/O		USB0_DP		

143	RESETN	I/O	BGPIO_Z_01(ALT0)RESETN(ALT1)TAMP_01(ALT2)SOC_PZ_01(ALT3)	PZ01		
144	WBUTN	I/O	BGPIO_Z_03(ALT0)WBUTN(ALT1)TAMP_03(ALT2)SOC_PZ_03(ALT3)	PZ03		
145	VBAT	I		VBAT		
146	PLED	I/O	GPIO_Z_04(ALT0)GPTMR7_CAPT_0(ALT1)UART11_RXD(ALT2)SPI0_MOSI(ALT5)I2S0_FCLK(ALT8)PDM0_D_3(ALT10)	PZ04		
147	WLED	I/O	GPIO_Z_05(ALT0)UART11_TXD(ALT2)SPI0_MISO(ALT5)PDM0_D_2(ALT10)	PZ05		
148	BOOT1	I/O	BGPIO_Z_07(ALT0)TAMP_07(ALT2)SOC_PZ_07(ALT3)	PZ07		
149	JTAG_TDO	I/O	PGPIO_Y_00(ALT0)JTAG_TDO(ALT1)PTMR_COMP_0(ALT2)SOC_PY_00(ALT3)	PY00		
150	CAN0_STBY	I/O	GPIO_Y_05(ALT0)GPTMR6_CAPT_1(ALT1)UART5_CTS(ALT3)I2C3_SDA(ALT4)SPI1_CSN(ALT5)CAN0_STBY(ALT7)DAOL_N(ALT10)ACMP_COMP_0(ALT16)	PY05		
151	UART0_TX	I/O	GPIO_Y_06(ALT0)UART0_TXD(ALT2)CAN1_TXD(ALT7)I2S1_TXD_0(ALT8)	PY06		

152	GND	G				
153	GND	G				
154	GND	G				
155	GND	G				
156	3V3	P				
157	GND	G				
158	U6_UART0_RX	I/O	GPIO10 is high, GPIO6→UART_TX1, GPIO7→UART_RX1			18 (GPIO7)
159	U6_UART0_TX	I/O				19 (GPIO6)
160	3V_BCKP2	I	It is advisable to externally connect a decoupling capacitor to the input terminal of the backup power supply, and during PCB layout , ensure that the capacitor (>1uF) is situated close to the corresponding pin			6 (VBCKP)
161	3V3	P				
162	GND	G				
163	3V3	P				
164	GND	G				
165	3V3	P				
166	U5_UART0_TX	I/O	GPIO10 is high, GPIO6→UART_TX1, GPIO7→UART_RX1		18 (GPIO7)	
167	U5_UART0_RX	I/O			19 (GPIO6)	
168	3V3	P				
169	GND	G				
170	3V3	P				

Appendix - Revision History

VERSION	REVISION	Release Date
V1.0	first release	2024.11.26
V1.1	Modify the schematic diagram of the packaged product, and add relevant content on the microsystem chip architecture and pin definition	2025.07.30

BW-GIP200 series

Seven-axis Integrated Navigation

Wuxi BWSENSING Technology Co.

Address: Building 30, No. 58 Xiuxi Road, Binhu

City

Hotline: 400-618-0510

Email: sales@bwsensing.com

Website: www.bwsensing.com.cn